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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,626	11/23/2005	Georg Bogner	5367-163PUS	2021
27799	7590	09/11/2006	EXAMINER	
COHEN, PONTANI, LIEBERMAN & PAVANE 551 FIFTH AVENUE SUITE 1210 NEW YORK, NY 10176			ARORA, AJAY	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No. 10/529,626	Applicant(s) BOGNER ET AL.	
	Examiner Ajay K. Arora	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 3/30/05 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/30/05 (two)</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 5.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9, 10, 16, 22, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Harrah (6,498,355), hereinafter Harrah.

Regarding claim 1, Harrah (refer to Figure 2-4) teaches an optoelectronic component having a semiconductor arrangement (28) which emits and/or receives electromagnetic radiation and which is arranged on a carrier (30) which is thermally conductively connected (using 24) to a heat sink (6), and having external electrical connections (42/44) which are connected to the semiconductor arrangement (28), wherein the external electrical connections (42/44) are arranged in electrically insulated fashion (by dielectric layers 10 and 48) on the heat sink (6) at a distance from the carrier (30).

Regarding claim 2, Harrah (refer to Figure 2-4) teaches that the carrier (30) contains a carrier substrate and at least one electrically insulating layer (Col. 4, lines 51-54) arranged thereon.

Regarding claim 3, Harrah (refer to Figure 3) teaches the semiconductor arrangement (28) and the electrically insulating layer (Col. 4, lines 51-54) have an electrically conductive layer (layer to which wire bonds 48 or 50 are attached closest to

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semiconductor arrangement 28) arranged between them which is connected to one of the external electrical connections.

Regarding claim 4, Harrah (refer to Figures 2-4) teaches that the semiconductor arrangement (28) contains a semiconductor chip (Col. 2, lines 57-60).

Regarding claim 5, Harrah (refer to Figure 4) teaches that the external electrical connections (42/44) include conductor tracks (8) on a printed circuit board (52).

Regarding claim 6, Harrah (refer to Figure 4) teaches that conductor tracks (8) on different printed circuit boards (Col. 6, lines 33-37) arranged above one another can be connected to one another by means of plated-through holes (that form vias 12).

Regarding claim 7, Harrah (refer to Figures 2-4) teaches the carrier (30) substrate has at least one material with good thermal conductivity from the group comprising Si (Col. 4, lines 51-54), diamond-coated Si, diamond, SiC, AlN and BN.

Regarding claim 9, Harrah (refer to Figures 2-4) teaches that the semiconductor arrangement (28) is attached to the carrier (30) by means of a metal solder (32).

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Regarding claim 10, Harrah (refer to Figures 2-4) teaches that the carrier (30) is attached to the heat sink (6) by means of a metal solder or a thermally conductive (Col. 5, lines 1-7) adhesive (24).

Regarding claim 16, Harrah (refer to Figures 2-4) teaches that the semiconductor arrangement (28) is at least partly encapsulated by a radiation-pervious encapsulation compound (26).

Regarding claim 22, Harrah teaches a component-based module, wherein it has plurality of optoelectronic components as claimed in claim 1 (Col. 4, lines 36-38).

Regarding claim 25, Harrah teaches the component-based module as claimed in claim 22, wherein a plurality of optoelectronic components each have a basic housing (26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah in view of Jackson (US 6,800,930), hereinafter Jackson.

Regarding claim 8, Harrah (refer to Figures 2-4) teaches substantially the claimed structure including the electrically insulating layer but does not teach that the electrically insulating layer comprises SiO₂. Jackson teaches the use of electrically insulating layer comprising SiO₂ (Col. 6, lines 55-58). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the electrically insulating layer comprises SiO₂. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of utilizing a dielectric that has excellent adhesion to chips and substrates that often comprise silicon.

Claims 11-13, 15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah in view of Komoto (US 6,340,824), hereinafter Komoto.

Regarding claim 11, Harrah (refer to Figures 2-4) teaches the semiconductor arrangement (28) and the carrier (30) are arranged in basic housing (26), but does not teach that the basic housing comprises a "cavity" and that the semiconductor arrangement and the carrier are arranged in "the cavity of a basic housing". Komoto (refer to Figure 10C) teaches an optoelectronic component with a semiconductor arrangement (10 or 50) in a cavity of the basic housing (Col. 19, lines 35-39). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the semiconductor arrangement and the carrier are arranged in the cavity of a basic housing. The ordinary artisan would have been

motivated to modify Harrah for at least the purpose of providing a cavity instead of an area filled completely with resin to limit the attenuation of the LED light say by impurities in the resin.

Regarding claim 12, Harrah (refer to Figures 2-4) as modified above teaches that the cavity of the basic housing (26) contains precisely one semiconductor arrangement (28).

Regarding claim 13, Harrah teaches substantially the claimed structure but does not teach that the basic housing "is formed at an angle on the inner side" which faces the semiconductor arrangement, so that the basic housing has a reflective area" for a portion of the radiation emitted by the semiconductor arrangement. Komoto (refer to Figure 10C) teaches an optoelectronic component with a semiconductor arrangement (10 or 50), wherein the basic housing (520) is formed at an angle on the inner side which faces the semiconductor arrangement (10 or 50), so that the basic housing has a reflective area (Col. 19, lines 41-44) for a portion of the radiation emitted by the semiconductor arrangement. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the basic housing is formed at an angle on the inner side which faces the semiconductor arrangement, so that the basic housing has a reflective area for a portion of the radiation emitted by the semiconductor arrangement. The ordinary artisan would have

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been motivated to modify Harrah for at least the purpose of providing control of light intensity in a specific direction depending on the angle of the reflective area.

Regarding claim 15, Harrah teaches substantially the claimed structure but does not teach that the filling compound contains TiO_2 or an epoxy resin filled with TiO_2 particles. Komoto (refer to Figure 106) teaches an optoelectronic component, wherein the filling compound (2140a) contains TiO_2 or an epoxy resin filled with TiO_2 particles (Col. 48, lines 66-67). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the filling compound contains TiO_2 or an epoxy resin filled with TiO_2 particles. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing wavelength selectivity (see Komoto, Col. 48, lines 24-34).

Regarding claim 17, Harrah (refer to Figures 2-4) teaches at least some of the external connections (42/44) are arranged between the basic housing (26) and the heat sink (6).

Regarding claims 18, 19 and 20, Harrah teaches substantially the claimed structure but does not specifically teach that it is provided for an electrical power consumption of at least 0.5 W (per claim 18), at least 1 W (per claim 19), or at least 3 W (per claim 20). It would have been an obvious matter of design choice to one of ordinary skills in the art at the time of the invention to modify Harrah such that it is provided for an electrical power of at least 0.5 W, or 1 W, or 3 W respectively. Such design choices, for example

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increasing the size of heat sink, are routine in the art. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing a high light intensity while utilizing the heatsink for effective removal of dissipated heat.

Regarding claim 21, Harrah teaches substantially the claimed structure but does not specifically teach that the optoelectronic component has a base area of no more than 1 cm². It would have been an obvious matter of design choice to one of ordinary skills in the art at the time of the invention to modify Harrah such that the optoelectronic component has a base area of no more than 1 cm². The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing a high power output component with a relatively small footprint.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah in view of Komoto, and further in view of Salam (US 6,095,666), hereinafter Salam.

Regarding claim 14, Harrah teaches substantially the claimed structure but does not teach that "the cavity between the semiconductor arrangement and lateral walls of the cavity contains a reflective filling compound which, as seen from the semiconductor arrangement toward the front of the basic housing, has a curved surface which forms a reflective area for a portion of the radiation". Salam (refer to Figure 10) teaches LED package, which has a curved surface (58) which forms a reflective area for a portion of the radiation. Komoto (refer to Figure 46) teaches forming curved surfaces (surface of

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542E) filling compounds. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the cavity between the semiconductor arrangement and lateral walls of the cavity contains a reflective filling compound which, as seen from the semiconductor arrangement toward the front of the basic housing, has a curved surface which forms a reflective area for a portion of the radiation. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing control of light intensity in a specific direction (depending on the curvature of the reflective area) using a filling compound that can easily be shaped to various curvatures.

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah in view of Stopa (US 6,318,886), hereinafter Stopa.

Regarding claim 23, Harrah teaches substantially the claimed structure including component-based module having a plurality (Col. 4, lines 36-39) of optoelectronic components as claimed in claim 1, but does not specifically disclose that "at least some of the optoelectronic components are electrically conductively connected to one another by conductor tracks". Stopa teaches a module with plurality of optoelectronic components wherein at least some of the optoelectronic components are electrically conductively connected to one another by conductor tracks (Col. 5, lines 52-56). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that at least some of the optoelectronic components

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are electrically conductively connected to one another by conductor tracks. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of controlling at least some of the optoelectronic components together.

Regarding claim 24, Harrah teaches substantially the claimed structure including that the individual optoelectronic components are arranged in the form of a matrix (Col. 4, lines 36-39) but does not disclose that at least some of them are connected in series. Stopa teaches a module with plurality of optoelectronic components wherein at least some of the optoelectronic components are connected in series. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that at least some of the optoelectronic components are connected in series. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of supplying the same current to the optoelectronic components (since they are connected in series) to easily control one of the variables in the optoelectronic component light output.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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